ricetronics (Rice)

Intellectual Properties (IP) for 6G Application

The evolution of 6G communications faces numerous challenges. The availability of increased bandwidth alone does not ensure objectives of low latency, flexibility and high-performance. Accordingly ricetronics (Rice) targets multiple levels of IP to address these issues. The levels of IP may span networks, operational techniques, methods and circuits as depicted below:

I. Collaborative Multi-Tier Networking

Multi-tier Network including a Mobile millimeter wave (mmw) Network. The Mobile Network might share information with a higher-tier fixed Network through a Distributed Database containing status, spatial and velocity data of Users. Geo-spatial and multi-media information might also available for cross-network sharing

II. Ad Hoc Mobile Network

The Mobile Network might support point-to-point ad-hoc communications among Users without centralized control. Low-latency connectivity (e.g., tens of microseconds) might be supported. Multi-domain access (time, space, code) may be employed to separate Users. Proprietary pulse train waveforms may containing both data and identification codes to facilitate separation of Users.

III. Subsystems, Structures and Circuits

Rice IP developments and objectives are to enable 6G ad hoc networks, and intelligent platforms employing said networks. The IP might span waveforms, structures, methods, subsystems and circuits. These may include;

- specialized waveforms and waveform generators,
- wide-bandwidth modulators/demodulators,
- phase-controlled beamformers,
- specialized processors.

These may comprise critical building blocks for advanced “physical layers” of future RF networks. Additionally, specialized processors might imbue Users of said networks with unique computing capability for tasks such as pattern recognition and multi-media processing. An overview of various structures, methods and circuits is presented below.

Circuits, Methods and Waveforms

Rice IP developments may include circuits, methods and waveforms for future 6G RF systems. Waveforms may include both OFDM and proprietary spread spectrum formats, and might be used to trade-off detectability versus data capacity over a range of scenarios. Minimization of Peak-to-Average-Power Ratio (PAPR) is inherent in the waveform approaches. Shown in Figure 1, a waveform might take the form of a pulse having intricate internal content, (as opposed to a simple “Ultra Wideband” or “UWB” pulse). Multiple pulses may be used to construct a “pulse train”.

Waveforms

Internal features of an individual pulse might be complex as shown at the bottom of Figure 1. Both data and codes might be embedded into the pulse. The Figure depicts a time-sampled version of a pulse, as may be consistent with certain discrete processing methods. The pulse train may also be characterized by a specific Pulse Rate Interval (PRI), as indicated in Figure 1.

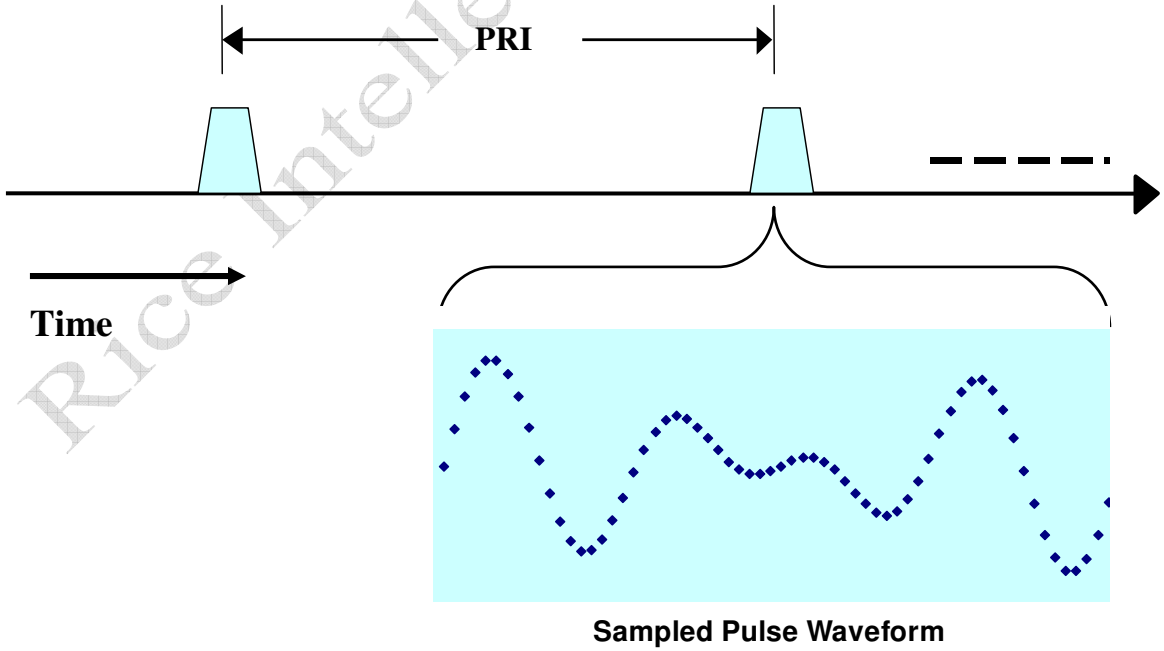


FIG. 1

Rice Intellectual Property includes methods and electronic circuits for generation and modulation of pulse waveforms. Circuits are optimized to meet the severe size and cost limitations of internet-of-things (IoT) and machine-to-machine (M2M) applications. Also, novel methods can produce pulse waveform power levels of an almost uniform probability distribution. This is a distinct advantage in the transmission of intricate RF waveforms. It mitigates issues of elevated PAPR levels, which may quickly diminish battery life in certain applications. These may range from personal communications to IoT scenarios. The pulse waveforms might have certain proprietary construction, but also share advantages of traditional signal formats such as OFDM and SC-OFDM. The pulses might combine User data, “correction data” as well as identification codes, to separate a multiplicity of Users in a pulse communications Network.

Modulators / Demodulators

The Rice IP extends to certain modulators and demodulators for processing of wide-bandwidth signals. These structures might operate upon a variety of signal formats, including OFDM, SC-OFDM and a variety of proprietary signal structures.

The modulators / demodulators may include high-speed Discrete Fourier Transform (DFT) processing structures, supported by various interfaces, pre-processors and post-processors. These DFT structures might be optimized for execution of smaller transform sized. Further, they might be implemented by either conventional digital circuitry, or in-memory computing circuit elements.

Discrete Fourier Transform (DFT)s

A particular area of Rice research is advanced circuit structures for Fourier analysis. Within this area are highly efficient structures for computation of Discrete Fourier Transforms (DFTs). The classical equation defining the DFT is given as:

$$F(j) = \sum_{n=0}^{M-1} f(n) \mathrm{W}^{jn}$$

where;

f(n) is an input sequence to the DFT,
W is the complex exponential = $e^{-(2\pi i)/M}$
M = transform length
j is an index on the DFT outputs
n is an index on the DFT inputs.

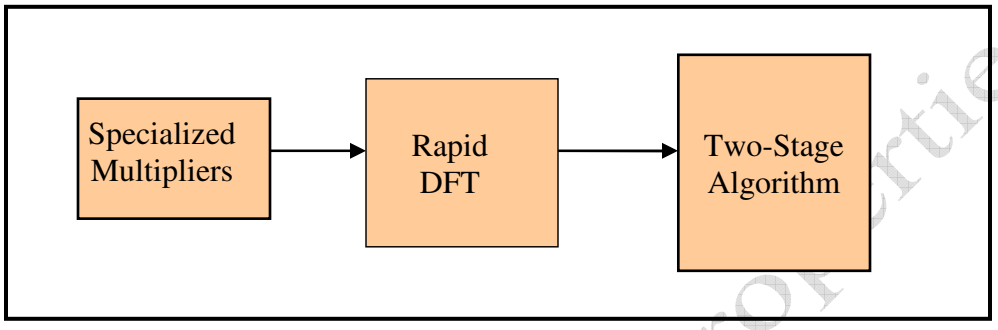
Multiplication operations typically drive the complexity of high-performance circuitry in "direct" DFT evaluation. Direct (brute force) evaluation of the above expression might require M^2 multiplications (for example, if f(n) is a real-valued sequence).

However, the IP may define processes and structures for highly efficient computation of "small" DFTs. This may be based upon two custom approaches. The first is specialized circuitry for multiplication by the complex exponential = $e^{-(2\pi i)/M}$ of the classic DFT expression above. Second is the exploitation of "Rapid DFTs", where certain computational redundancies of the classic DFT are eliminated.

The Rapid DFT might rival the efficiency of traditional FFT algorithms for small size transforms. At the same time, the Rapid DFT may be easier to implement than the FFT, due to more simplistic control and data movement characteristics.

The Rapid DFT might be used on a stand-alone basis for tasks including signal analysis, generation, modulation, demodulation and compression. Alternatively, the Rapid DFT may be used as a "building block" for larger size transforms. It is known from DSP theory that small DFTs might serve as the equivalent of large "butterfly" operations in the computation of large Fourier Transforms. A known approach is a "two-stage" algorithm

where small DFTs might be employed as large-radix butterflies within each stage. In this context the Rapid DFT might be used as a butterfly in the construction of massive Fourier Transforms. Accordingly, Figure 2 depicts a design hierarchy where the Rice IP may be used at different levels to optimize the cost/performance characteristics of large FFTs.



Large FFT Design Hierarchy

FIG. 2

As suggested in Figure 2, the two-stage algorithm might be efficiently executed using the Rapid DFT as a building block. Further, the physical design of the Rapid DFT might be optimized by use of circuits specialized for multiplication by the complex exponential functions of the DFT. This may render very large transforms which are comparable in performance to traditional FFTs, but at a small fraction of the circuit complexity. A customized implementation of the two-stage algorithm might be orders of magnitude less complex than that implemented with an FPGA or a graphics processor.

Beamformer Structures and Methods

The Rice IP extends to various beamforming structures and methods. These are devised to support the wide bandwidths and high carrier frequencies of 6G signals. Further, they enable the intricacies of phase control beamforming.

The physics of beamforming involves either adjustable time delays of multiple RF antenna signal paths, or phase control within such paths. Phase controlled beamformers

are generally classified as either analog, digital or hybrid. Of these three options, digital phase control is preferable for precise spatial beam formation, switching and steering. However digital phase control of a multiplicity of signal paths is often not feasible for small, low-cost form factors. This is due to the need for complex digital circuitry and a multiplicity of signal conversion (A/D and D/A) devices.

The Rice IP may provide operational advantages of digital beamforming with reduced circuit cost and complexity. The massive A/D and D/A circuitry normally required for digital beamforming may be obviated by the unique IP methods and structures. These include the novel use of in-memory computing to achieve the benefits of digital phase controlled beamforming, but with far less circuitry and power consumption.

Memristors are a type of in-memory computing element which can be fabricated in high densities with low power consumption. The IP may configure memrisors in a multiplicity of antenna signal paths to effect beamforming with large antenna arrays. Magnitude and phase responses of signal paths may be independently controlled. This represents a novel application of memristor technology, enabling highly agile formation and precision pointing of a multiplicity of RF beams.

Additional challenges to beamforming include “beam squint”. This phenomenon can substantially distort the effective gain pattern of the beamformer antenna array. This can result in a serious decrease in data link capacity. The deleterious effects of beam squint can become even more pronounced with higher carrier frequencies and wide-bandwidths of 6G signals. Therefore it is a another significant aspect of the beamforming IP, that beam squint may be mitigated by employment of the in-memory computing methods and structures.

Although memristor technologies have been researched for neural networks, their acceptance has been slowed by various characteristics. However, the structures and methodologies of the IP serve to resolve several of these traditional limitations.

Summary

Rice IP and areas of interest spans the range of systems to circuits. The IP encompasses innovative concepts and technologies for future high-bandwidth communications and computing systems. Objectives of the IP are to enable fundamentally new solutions to fundamental engineering challenges.

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